

FORM PTO-1449	ATTY. DKT NO.	01-149-DIV	SER. NO.	10/786,107
	APPLICANT ITO et al.			
	FILING DATE	February 26, 2004	GROUP	2822

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
JMJ	5,448,083	09-1995	Kitagawa et al.		
	6,110,799	08-2000	Huang	438	430
	5,895,951	04-1999	So et al.	257	330
	6,213,869	04-2001	Yu et al.	458	236
	5,998,836	12-1999	Williams		
	5,072,266	12-1991	Bulucea et al.		
	6,049,108	04-2000	Williams		
	6,140,678	10-2000	Grabowski et al.		
JMJ	5,907,776	05-1999	Hshieh et al.	438	270

FOREIGN PATENT DOCUMENTS

TRANSLATION								
	DOCUMENT NUMBER	DATE	COUNTRY	NAME	CLASS	SUB CLASS	YES	NO
								Eng. Abstract
JMJ	JP-A-5-206264	8/13/94	JAPAN					X
	JP-A-5-226351	9/3/93	JAPAN					X
	JP-A-6-151867	5/31/94	JAPAN					X
	JP-A-7-249770	9/26/95	JAPAN					X
	JP-A-8-264772	10/11/96	JAPAN					X
JMJ	JP-B2-2590863	Published on 9/19/88	JAPAN					X

* Full English text of the JP Document will be available in machine-translated form from JP (Japanese Patent Office) English language web site at <http://www1.ipdl.jpo.go.jp/PA1/cgi-bin/PA1INDEX>.

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

JMJ	S. Wolf, "Silicon Processing for the VLSI Era," Volume 2 - "Process Integration," Lattice Press (Sunset Beach, CA), ISBN 0-961672-4-5 (1990); particularly pages 658-663.
EXAMINER	DATE CONSIDERED
T. M. Thomas	06-25-05